Ch5

Processor Fundamentals

CHAPTER ASSIGNMENT · 63 MARKS

Name _____ Class _____ No. _____ Date _____

Answer every question in the space given. Show your working. You may use the chapter page to help you.

Questions from *Computer Science for Cambridge International AS & A Level Coursebook*, 2nd edition, Sylvia Langfield and Dave Duddell (Cambridge University Press), for classroom use.

Tasks and questions from the chapter

EQ5.01 **Extension Question 5.01:** In an advertisement for a laptop computer, the system is described as 4 GB, 1 TB, 1.7 GHz.

(a) Which three components are being referred to here?

(b) Calculate the minimum time period that could separate successive activities on this system.

EQ5.02 **Extension Question 5.02:** Can you find out the bus widths used in the computer system you are using?

DP **Discussion Point:** Carry out an investigation into storage devices that could be connected as a peripheral to a PC using the USB port.

For two representative devices find out which specific USB technology is being used and what the potential data transfer speed is. How do these speeds compare with the speed of access of a hard drive installed inside the computer?

DP **Discussion Point:** Carry out an investigation into the different causes of an interrupt.

RP **Reflection Point:** Have you worked out a method to remember all of the names and abbreviations for the special purpose registers?

Exam-style questions

1

(a) A processor has just one general-purpose register. Give the name of this register. [1]

(b) The memory address register (MAR) is a special-purpose register. State:

(i) its function

(ii) the type of data stored in it

(iii) the register that supplies these data at the start of the fetch stage of the fetch–execute cycle. [3]

(c) The current instruction register (CIR) is another special-purpose register. State:

(i) its function

(ii) the type of data stored in it

(iii) the register that supplies this data at the end of the fetch stage of the fetch–execute cycle. [3]

(d) Explain **three** differences between the memory address register and the memory data register. [5]

2 The system bus comprises of three individual buses: the data bus, the address bus and the control bus.

(a) For each bus give a brief explanation of its use. [6]

(b) Each bus has a defined bus width.

(i) State what determines the width of a bus. [1]

(ii) Explain which bus will have the least width. [2]

(iii) Explain the effect of changing the address bus from a 32-bit bus to a 64-bit bus. [3]

3 The fetch stage of the fetch–decode–execute cycle can be represented by the following statements using register transfer notation:

```
MAR ← [PC]
PC ← [PC] + 1; MDR [[MAR]]
CIR ← [MDR]
```

(a) Explain the meaning of each statement. The explanation must include definitions of the following items: MAR, PC, [ ], , MDR, [[ ]], CIR. [10]

(b) Explain the use of the address bus and the data bus for two of the statements. [4]

4

(a) Name and describe **three** buses used in the von Neumann model. [6]

(b) The sequence of operations shows, in register transfer notation, the fetch stage of the fetch-execute cycle.

```
1  MAR ← [PC]
2  PC  ← [PC] + 1
3  MDR ← [[MAR]]
4  CIR ← [MDR]
```

- `[register]` denotes contents of the specified register or memory location
- step 1 above is read as "the contents of the Program Counter are copied to the Memory Address Register"

(i) Describe what is happening at step 2. [1]

(ii) Describe what is happening at step 3. [1]

(iii) Describe what is happening at step 4. [1]

(c) Describe what happens to the registers when the following instruction is executed: [2]

`LDD 35`

(d) Explain what is meant by an interrupt. [2]

(i)

(ii) Explain the actions of the processor when an interrupt is detected. [4]

Cambridge International AS & A Level Computer Science 9608 paper 13 Q5 June 2015

5

(a) Describe how special purpose registers are used in the fetch stage of the fetch-execute cycle. [4]

(b) Use the statements A, B, C and D to complete the description of how the fetch-execute cycle handles an interrupt. [4]

A	the address of the Interrupt Service Routine (ISR) is loaded to the Program Counter (PC).
B	the processor checks if there is an interrupt.
C	when the ISR completes, the processor restores the register contents.
D	the register contents are saved.

At the end of the cycle for the current instruction .....

If the interrupt flag is set, ..., ... and .....

The interrupted program continues its execution.

End of assignment · Check your answers against the chapter at gurujazzy.com/subjects/computer-science/as-a-level/processor-fundamentals/